Notice of Allowability	Application No.	Applicant(s)	
	09/360,069	WOHL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Appeal Brief received 1/27/2005, and email 3/14/05*.

2. ☒ The allowed claim(s) is/are *37-53*.

3. ☒ The drawings filed on *23 July 1999* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

EXAMINER'S AMENDMENT and REASONS FOR ALLOWANCE

Introduction

1. Title is: METHOD AND SYSTEM FOR GENERATING AN ATPG MODEL OF A MEMORY FROM BEHAVIORAL DESCRIPTIONS
2. First named inventor is: WOHL
3. Applicant's Appeal Brief was received 1/27/05, and Applicants email with requested amendments was received 3/14/05.
4. Claims 37-53 are pending and are allowed.

Index of Important Prior Art and Dictionaries

5. **Cheng** refers to Gate-Level Test Generation for Sequential Circuits, by Kwang-Ting Cheng, ACM Transactions on Design Automation of Electronic Systems, Vol. 1, No. 4, October 1996, Pages 405-442.
6. **Beausang'771** refers to US Patent 5,696,771.
7. **"Using Verilog Simulation Libraries for ATPG"** refers to "Using Verilog Simulation Libraries for ATPG", 0-7803-5753-1/99 1999 IEEE, by Peter Wohl, and John Waicukauski (102a type prior art, and different inventive entity than present application).
8. **Tucker** refers to "The Computer Science and Engineering Handbook", by Allen B. Tucker, CRC Press, ISBN: 0-8493-2909-4, 1996, pages 450-453.
9. **Smith** refers to "HDL Chip Design" by Douglas J. Smith, 1996, Ninth printing 2001 minor updates, ISBN 0-9651934-3-8, pages 38-40.
10. **MS Dictionary** refers to Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.
11. **McGraw-Hill Dictionary** refers to The McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, by McGraw-Hill Companies, Inc., 2003, ISBN 0-07-042313-X.
12. **IEEE Dictionary** refers to The Authoritative Dictionary of IEEE Standards and Terms, Seventh Edition, by IEEE Press, ISBN 0-7381-2601-2, 2000.

Definitions

13. **"Associative memory"** is defined as "A type of memory whose locations are identified by their contents or by a part of their contents, rather than by their names or positions.

Synonyms: search memory, content addressable storage" by IEEE Dictionary. Note that Tucker page 450-453 states "The cache memory is associative, or content-addressable. In an associative memory, the address of a memory location is stored, along with its content. Rather than reading data directly from a memory location, the cache is given an address and responds by providing data which may or may not be the data requested. When a cache miss occurs, the memory access is then performed with respect to the backing storage, and the cache is updated to include the new data."

14. **"Automatic test pattern generator (ATPG)"** as "Any tool that generates test information for a device based on structural analysis of the device", by IEEE Dictionary.

15. **"Content addressable memory"** (CAM) is defined as "See: associative memory" by IEEE Dictionary.

16. **"Logical"** is defined as "Based on true and false alternatives as opposed to arithmetic calculation of numeric values... Boolean algebra", by MS Dictionary.

17. **"Primitive"** is defined as "[COMPUT SCI] A sketchy specification, omitting details, of some action in a computer program", by McGraw-Hill Dictionary.

18. **"Primitive"** is defined as "In programming, a fundamental element in a language that can be used to create larger procedures that do the work a programmer wants", by MS Dictionary.

19. **"Random access memory"** (RAM) is defined as "(1) A memory that permits access to any of its address locations in any desired sequence with similar access time to each location (adapted from IEC 748-2). Note: The term RAM, as commonly used, denotes a read/write memory with unlimited data rewrite capability and equal read and write times." by IEEE Dictionary.

Examiner's Amendment

20. The Examiner hereby amends the claims according to said email, which is attached with a clean copy of the amended claims, per MPEP 13.02.04.

21. Note that said clean copy contains claims 37-53, which are allowed, and all other claims are cancelled.

22. See attached email, per MPEP 13.02.04:

As an alternative, the examiner's amendment utilizing paragraph/claim replacement can be

created by the examiner with authorization from the applicant. The examiner's amendment can also be created from a facsimile transmission or e-mailed amendment received by the examiner and referenced in the examiner' s amendment and attached thereto. Any subject matter, in clean version form (containing no brackets or underlining), to be added to the specification/claims should be set forth separately by applicant in the e-mail or facsimile submission apart from the remainder of the submission. A clean version of a paragraph/claim, or portion of a paragraph/claim, submitted by applicant in a fax or e-mail, should be printed and attached to the examiner's amendment and may be relied on as part of the examiner's amendment. The examiner should mark "requested" on the entire attachment to indicate that the fax or e-mail was requested by the examiner, so as to not lead to a reduction in patent term adjustment (37 CFR 1.704(c)(8)). As the attachment is made part of the examiner's amendment, it does not get a separate PALM code and will not trigger any reduction in patent term adjustment. A paper copy of the entire e-mail or facsimile submission should be entered in the application file. Examiners are not required to electronically save any e-mails once any e-mails or attachments thereto are printed and become part of an application file record. The e-mail practice that is an exception for examiner's amendments is restricted to e-mails to the examiner from the applicant and should not be generated by the examiner to the applicant unless such e-mails are in compliance with all of the requirements set out in MPEP § 502.03.

Reasons for Allowance

23. In claim 37, the individual specific primitives are disclosed in the prior art. However, no prior art anticipates or makes obvious the claimed primitives in the claimed arrangement. All other claims are allowed for the same reasons.

Conclusions

24. All pending claims are allowed, specifically claims 37-53. All prior objections and rejections are withdrawn.

Communication

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 571-272-3711. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, then any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. For emergencies, the Examiner's supervisor, Kevin Teska, can be reached at 571-272-3761. The fax phone number for this group is 703-872-9306.

* * * *

KEVIN L. TESKA
SUPERVISORY
PATENT EXAMINER

REQUESTED

Garcia-Otero, Eduardo

From: Jeanette S. Harms [jharms@BeverLaw.Com]
Sent: Monday, March 14, 2005 1:59 PM
To: Garcia-Otero, Eduardo
Cc: Becky Baumann
Subject: SYN-0136

SYN-0136 Clean Set Of Claims O...

Dear Examiner Garcia-Otero:
It was a pleasure speaking with you this morning. Per our telephone conversation, I am attaching a clean set of claims including requested amendments for Claims 37-53. Please let me know if there is anything else you need from me to ensure allowance of this case.
Best regards,
Jeanette Harms

<<SYN-0136 Clean Set Of Claims On Appeal.doc>>

REQUESTED

SYN-0136

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Peter Wohl et al.

Assignee: Synopsys, Inc.

Title: METHOD AND SYSTEM FOR GENERATING AN ATPG MODEL OF A MEMORY FROM BEHAVIORAL DESCRIPTIONS

Serial No.: 09/360,069 File Date: July 23, 1999

Examiner: Eduardo Garcia-Otero Art Unit: 2123

Docket No.: SYN-0136(RCE)

Date: March 14, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CLEAN SET OF CLAIMS INCLUDING REQUESTED AMENDMENTS

37. A memory model usable for computer simulation and automatic test pattern generation, the memory model comprising:

a memory primitive comprising a write_address port, a write_data port, and an output port;

a read data port primitive comprising a read_data port for coupling to the output port of the memory primitive, a read_address port, and an output port;

an address bus primitive comprising an output port for coupling to the write_address port of the memory primitive and the read_address port of the read data port primitive;

a data bus primitive comprising an output port for coupling to the write_data port of the memory primitive; and

a plurality of memory out primitives, each memory out primitive comprising an input port for coupling to the output port of the read data port primitive.

REQUESTED

38. The memory model of Claim 37, wherein the memory primitive further includes:

a set input port;

a reset port;

a write_clock port; and

a write_enable port.

39. The memory model of Claim 37, wherein the read data port primitive represents a read port functionality of the memory.

40. The memory model of Claim 39, wherein a dimension of the output port of the read data port corresponds to a data dimension of the memory primitive.

41. The memory model of Claim 37, wherein the address bus primitive represents an address functionality of a memory.

42. The memory model of Claim 41, wherein the address bus primitive includes:

a plurality of input ports corresponding to an address dimension of the memory primitive.

43. The memory model of Claim 42, wherein the address bus primitive further includes an attribute indicating whether an incoming address is encoded or decoded.

44. The memory model of Claim 43, wherein the data bus primitive represents a data bus functionality of the memory.

REQUESTED

45. The memory model of Claim 44, wherein the data bus includes:

a plurality of input ports corresponding to a data dimension of the memory primitive.

46. The memory model of Claim 37, wherein each memory out primitive represents a simulated value storage functionality of the memory.

47. The memory model of Claim 37, wherein each memory out primitive includes an output port.

48. The memory model of Claim 47, wherein a plurality of tristate drivers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

49. The memory model of Claim 47, wherein a plurality of edge-triggered registers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

50. The memory model of Claim 49, wherein input ports of a plurality of tristate drivers can be coupled to output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive.

51. A content addressable memory model usable for computer simulation and automatic test pattern generation, the content addressable memory model comprising:

a memory primitive including an output port;

REQUESTED

a compare port primitive including a data port for coupling to the output port of the memory primitive, a data bus port, and an output port;

a data bus primitive including an output port for coupling to the data bus port of the compare port primitive;

a plurality of memory output primitives, each memory output primitive including an input port for coupling to the output port of the compare port primitive and an output port; and

an address bus primitive including input ports for coupling the output ports of a set of the memory output primitives.

52. The content addressable memory model of Claim 51, wherein the compare port primitive further includes:

a compare enable port for receiving a compare signal.

53. A combined content addressable memory (CAM) and random access memory (RAM) model usable for computer simulation and automatic test pattern generation, the combined CAM and RAM model comprising:

a first memory primitive including an output port;

a data bus primitive including an output port;

a compare port primitive for coupling to the memory primitive and the data bus primitive, the compare port primitive comprising;

a compare enable port;

a data bus port for coupling to the output port of the data bus primitive;

a data port for coupling to the output port of the first memory primitive; and

an output port;

REQUESTED

a first plurality of memory output primitives, each memory output primitive including an output port and an input port for coupling to the output port of the compare port primitive;

an address bus primitive including an output port and input ports for coupling to output ports of a first subset of the first plurality of memory output primitives;

a second memory primitive including an output port;

a read data port primitive including a first input port for coupling to the output port of the second memory primitive, a second input port for coupling to an output port of the address bus primitive, and a third input port for coupling to the output ports of a second subset of the plurality of memory output primitives; and

a second plurality of memory output primitives, each memory output primitive including an input port for coupling to an output port of the read data port primitive.